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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/551,837	10/03/2005	Soha M. N. Hassoun	TUFTS-002AUS	4243
22494 7590 06/02/2008 DALY, CROWLEY, MOFFORD & DURKEE, LLP SUITE 301A 354A TURNPIKE STREET CANTON, MA 02021-2714			EXAMINER TAT, BINH C	
			ART UNIT 2825	PAPER NUMBER
			NOTIFICATION DATE 06/02/2008	DELIVERY MODE ELECTRONIC

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

docketing@dc-m.com  
amk@dc-m.com

<b>Office Action Summary</b>	<b>Application No.</b> 10/551,837	<b>Applicant(s)</b> HASSOUN ET AL.	
	<b>Examiner</b> BINH C. TAT	<b>Art Unit</b> 2825	

**-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --**

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 13 February 2008.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 13-22 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 13-22 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 13 February 2008 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some \*    c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)          | 4) <input type="checkbox"/> Interview Summary (PTO-413)           |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____                                      |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)          | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____  | 6) <input type="checkbox"/> Other: _____                          |

### **DETAILED ACTION**

1. This office action is in response to amendment file on 02/13/08.

#### ***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

2. Claims 13-22 are rejected under 35 U.S.C. 102(a) as being anticipated by Robertson W et al.: "RTL synthesis for systolic arrays" Proceedings of the international symposium on circuit and system (ISCS). CHICAGO, MAY 3 - 6, 1993, NEW YORK, IEEE, US, vol. VOL. 2, 3 May 1993 (1993-05-03), pages 1670-1673, XP010115439 ISBN: 0-7803-1281-3
3. As to claim 13, Ashar et al. teach a method of scheduling processing in a hardware threaded circuit, comprising: receiving inputs corresponding to unthreaded processing of an application (see page 1670 col 1, line 8 to page 1670 col 2 line 4 and abstraction); receiving information including processing element resources, a number of processing elements, and a window size corresponding to a number of downstream processing states to be examined (see page 1671, col 2 line 20 to 1672 col 2 line 50); and generating a hardware threaded schedule for processing the application with at least first and second one of the processing elements being interconnected to enable dynamic resource sharing (see page 1670 col 2 line 7 to page 1671 col 1 line 35).
4. As to claim 14, Ashar et al. teach further including synthesizing the hardware threaded schedule to an Application Specific Circuit (ASC) (see page 1671 col 1 line 8-35).

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5. As to claim 15, Ashar et al. teach further including synthesizing the hardware schedule to maximize throughput (see page 1671 col 1 line 8-35).
6. As to claim 16, Ashar et al. teach further including synthesizing the hardware threaded schedule to reduce power consumption (see page 1672 col 1 line 20 to page 1672 col 2 line 50).
7. As to claim 17, Ashar et al. teach further including receiving resource constraint information for the processing elements (see page 1672 line 18 to page 1673 col 2 line 15).
8. As to claim 18, Ashar et al. teach a hardware threaded circuit system, comprising: a memory (see page 1670 col 1, line 8 to page 1670 col 2 line 4 and abstraction); a task manager coupled to the memory (see page 1671, col 2 line 20 to 1672 col 2 line 50); and a plurality of processing elements coupled to the task manager, wherein first and second ones of the plurality of processing elements are interconnected for hardware threaded processing to enable dynamic borrowing of processing resources associated with the second one of the plurality of processing elements by the first one of the plurality of processing elements (see page 1670 col 2 line 7 to page 1671 col 1 line 35).
9. As to claim 19, Ashar et al. teach wherein the circuit maximizes throughput (see page 1671 col 1 line 8-35).
10. As to claim 20, Ashar et al. teach wherein the circuit reduces power consumption compared to a non-threaded processing for substantially similar system wait times (see page 1672 col 1 line 20 to page 1672 col 2 line 50).
11. As to claim 21, Ashar et al. teach wherein the first and second processing elements each include a first type of resource and a second type of resource and a multiplexer such that the

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interconnection includes at least one input signal being provided to the first type of resource in the first and second processing elements (see page 1670 col 2 line 7 to page 1671 col 1 line 35).

**12.** As to claim 22, Ashar et al. teach wherein the interconnection includes a connection from an output of the second processing element first type of resource to the first processing element (see page 1670 col 2 line 7 to page 1671 col 1 line 35).

### ***Conclusion***

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Any inquiry concerning this communication or earlier communications from the examiner should be directed to Binh C. Tat whose telephone number is 571 272-1908. The examiner can normally be reached on 7:30 - 4:00 (M-F).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on 571 272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Binh Tat  
Art unit 2825

/Thuan Do/  
Primary eExaminer., Art Unit-2825  
05/26/2008